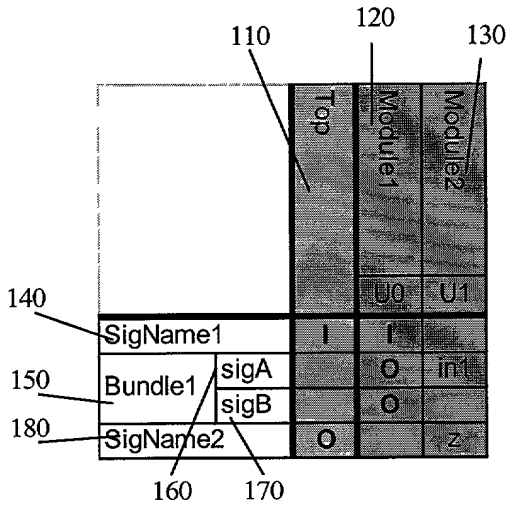



Figure 1

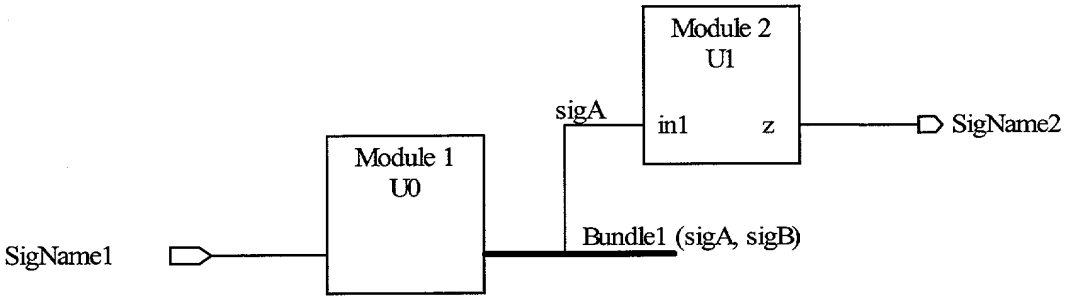



**Figure 2**

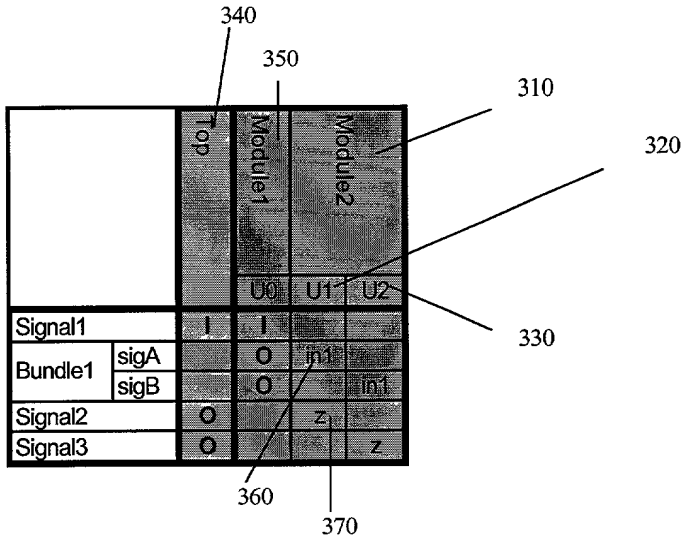



Figure 3

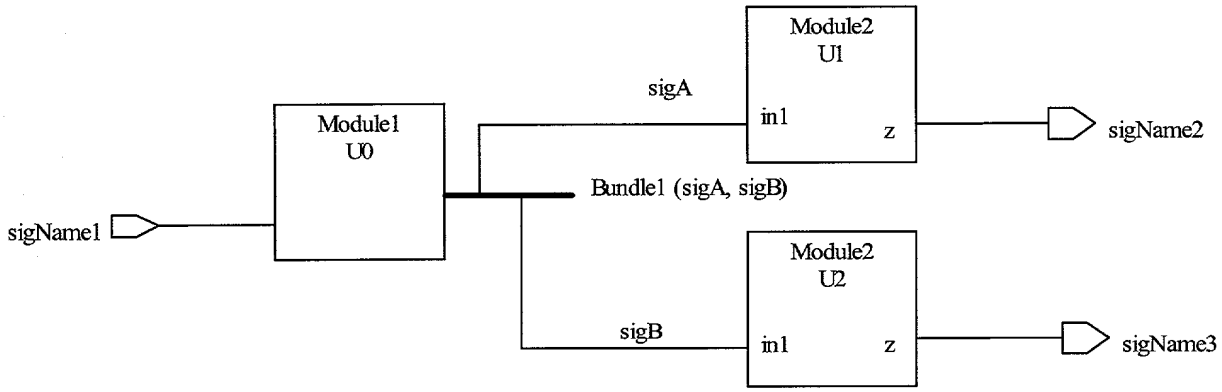



Figure 4

```
503  LIBRARY ieee;
504  USE ieee.std_logic.all;
505
506  ENTITY Top IS
507          port    (Signal1 : IN std_logic;
508                   Signal2 : OUT std_logic
509                   Signal3 : OUT std_logic);
510  END Top;
511
512  ARCHITECTURE struct OF Top IS
513
514      SIGNAL sigA             : std_logic;
515      SIGNAL sigB             : std_logic;
516
517      COMPONENT Module1
518      PORT(
519          Signal1      : IN std_logic;
520          sigA         :OUT std_logic;
521          sigB         :OUT std_logic;
522      );
523      END COMPONENT;
524
525      COMPONENT Module2
526      PORT(
527          in1    : IN    std_logic;
528          z      : OUT std_logic;
529      );
530      END COMPONENT;
531
532  BEGIN
533
534      U0 : Module1
535          PORT MAP(
536              sigA      => sigA,
537              sigB      => sigB,
538              Signal1   => Signal1
539          );
540
541      U1 : Module2
542          PORT MAP(
543              in1 => sigA,
544              z   => Signal2
545          );
546
```

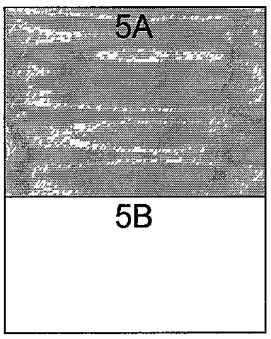



Figure 5

Figure 5A

```
546         U2 : Module2
547             PORT MAP(
548                 in1 => sigB,
549                 z   => Signal3
550             );
551
552
553 END ARCHITECTURE struct;
554
```

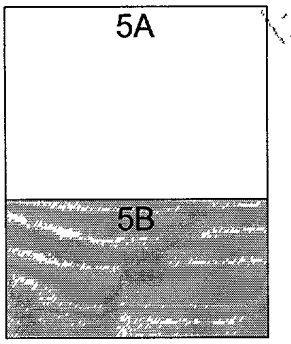



Figure 5

Figure 5B

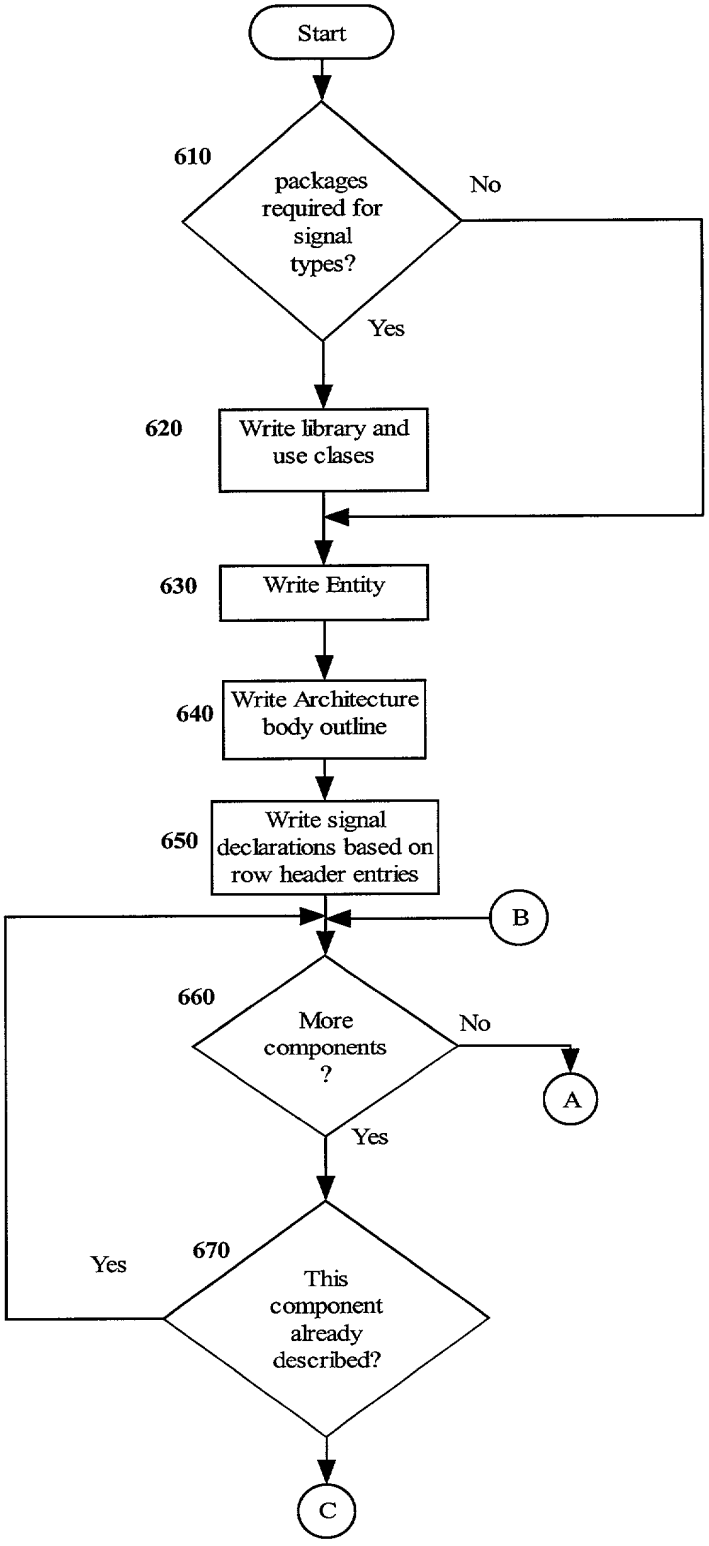

Start
610
packages required for signal types?
No
Yes
620
Write library and use clases
630
Write Entity
640
Write Architecture body outline
650
Write signal declarations based on row header entries
B
660
More components ?
No
A
Yes
670
Yes
This component already described?
C

Figure 6A

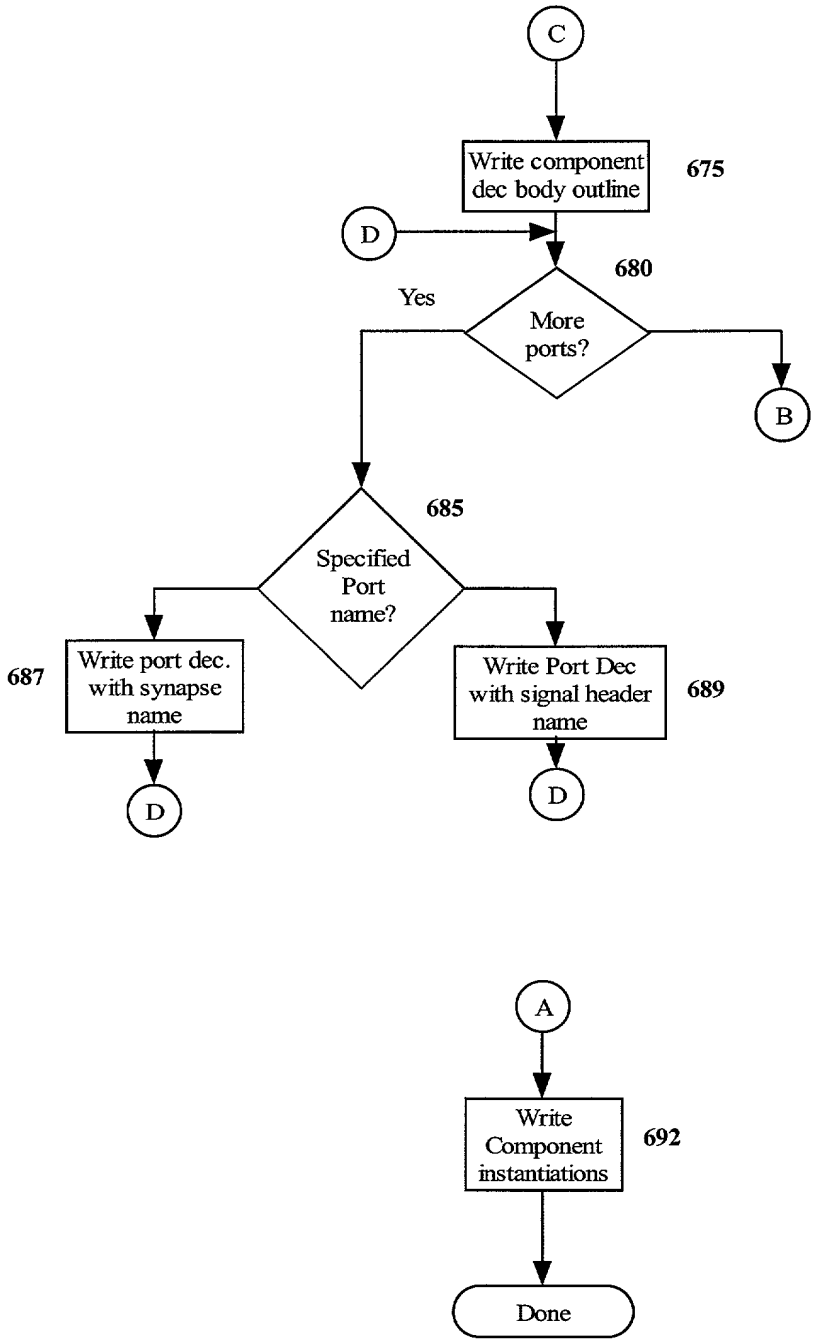

C
Write component dec body outline
675
D
680
Yes
More ports?
B
685
Specified Port name?
687
Write port dec. with synapse name
D
Write Port Dec with signal header name
689
D
A
Write Component instantiations
692
Done

Figure 6B

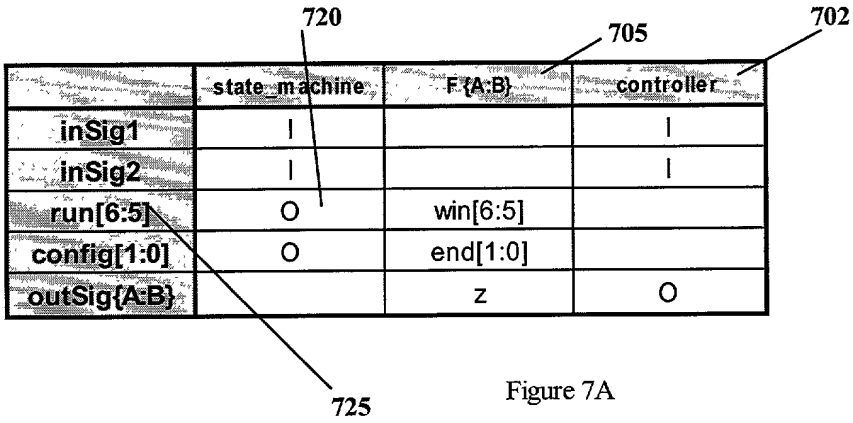



Figure 7A

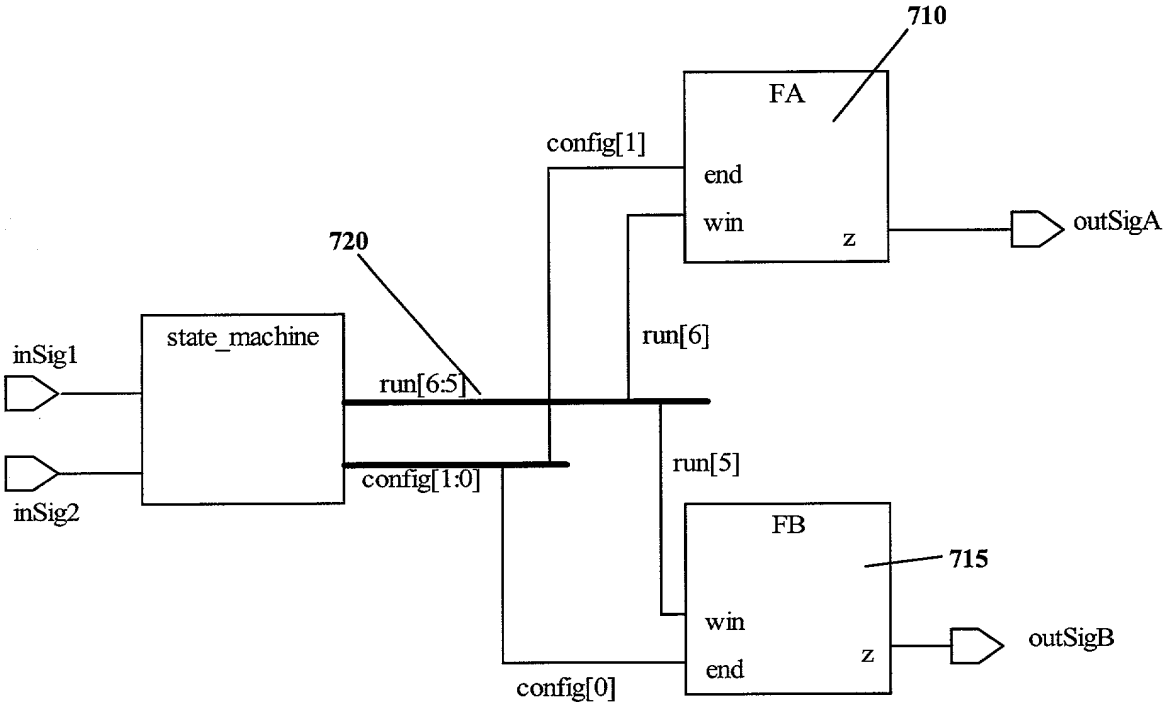



Figure 7B

| | Top | Module1 | Module2 | Delay | Comment |
|---|---|---|---|---|---|
| **in1** | I | I | | 20 ns | Input port for top |
| **intSig1** | | O | I | 10 ns | |
| **intSig2** | | O | I | 5 ns | |
| **out1** | O | | O | 5 ns | Output port for top |
| **cellName** | | Rev3 | | | |

Figure 8

```
LIBRARY ieee;
USE ieee.std_logic.all;

ENTITY Top IS
        PORT (in1    : IN    std_logic; -- Input port for top          910
              out1   : OUT std_logic); -- Output port for top          920
        ATTRIBUTE delay OF IN1 : SIGNAL IS 20 ns;                      930
        ATTRIBUTE delay OF OUT1 : SIGNAL IS 5 ns;                      940
END Top;

ARCHITECTURE struct OF Top IS

    SIGNAL intSig1          : std_logic;
    SIGNAL intSig2          : std_logic;
    ATTRIBUTE delay OF intSig1 : SIGNAL IS 10 ns;                      950
    ATTRIBUTE delay OF intSig2 : SIGNAL IS 5 ns;                       960


    COMPONENT Module1
    PORT(
        in1         : IN    std_logic;
        intSig1     : OUT std_logic;
        intSig2     : OUT std_logic;
    );
    END COMPONENT;

    ATTRIBUTE cellName of U0 : LABEL IS "Rev3";                        970

    COMPONENT Module2
    PORT(
        intSig1     : IN    std_logic;
        intSig2     : IN    std_logic;
        out1        : OUT std_logic;
    );
    END COMPONENT;

BEGIN

    U0 : Module1
        PORT MAP(
            in1     => in1,
            intSig1 => intSig1,
            intSig2 => intSig2
        );
```

Figure 9A

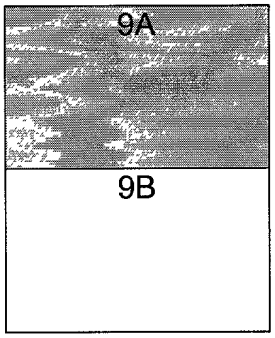



Figure 9

```
U1 : Module2
    PORT MAP(
        out1    => out1,
        intSig1     => intSig1,
        intSig2     => intSig2
    );

END ARCHITECTURE struct;
```

Figure 9B

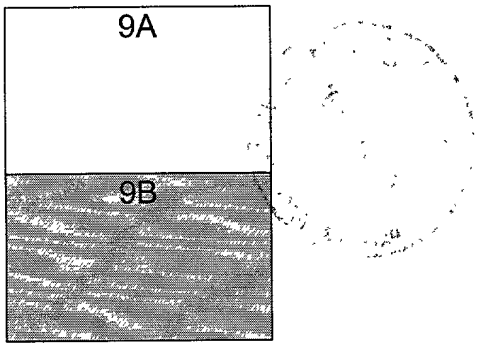
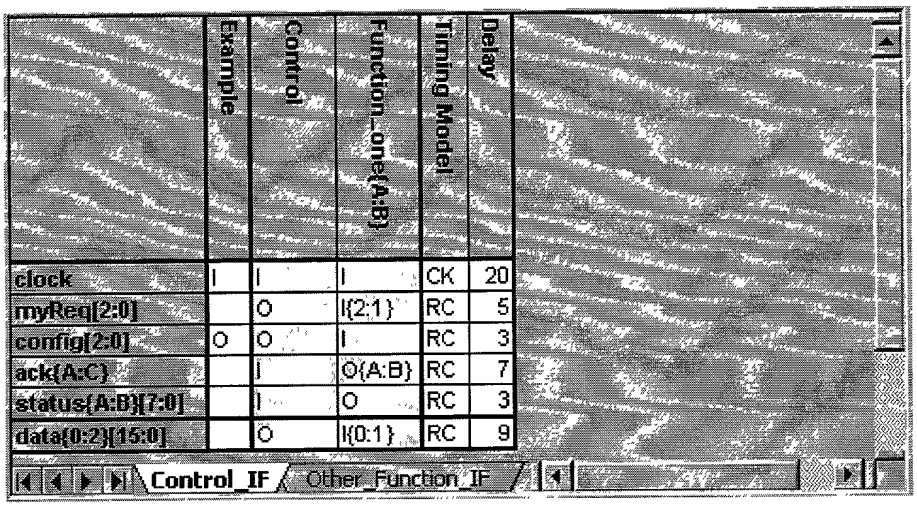


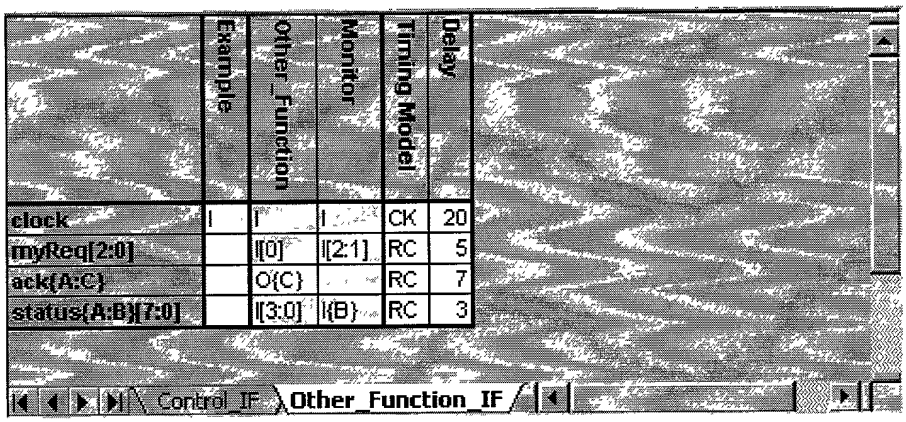

Figure 9



| | Example | Control | Function_one{A:B} | Timing Model | Delay |
|---|---|---|---|---|---|
| clock | I | I | I | CK | 20 |
| myReq[2:0] | | O | I{2:1} | RC | 5 |
| config[2:0] | O | O | I | RC | 3 |
| ack{A:C} | | I | O{A:B} | RC | 7 |
| status{A:B}[7:0] | | I | O | RC | 3 |
| data{0:2}[15:0] | | O | I{0:1} | RC | 9 |

Control_IF | Other_Function_IF

Figure 10



| | Example | Other_Function | Monitor | Timing Model | Delay |
|---|---|---|---|---|---|
| clock | I | I | I | CK | 20 |
| myReq[2:0] | | I[0] | I[2:1] | RC | 5 |
| ack{A:C} | | O{C} | | RC | 7 |
| status{A:B}[7:0] | | I[3:0] | I{B} | RC | 3 |

Control_IF | Other_Function_IF

Figure 11

| | Example | Control | Function_one{A:B} | Other_Function | Monitor | Check{2:0} | Timing Model | Delay |
|---|---|---|---|---|---|---|---|---|
| clock | I | I | I | I | I | I | CK | 20 |
| myReq[2:0] | | O | I{2:1} | I[0] | I[2:1] | | RC | 5 |
| config[2:0] | O | O | I | | | I[5:3] | RC | 3 |
| ack{A:C} | | I | O{A:B} | O{C} | | I | RC | 7 |
| status{A:B}[7:0] | | I | O | I[3:0] | I{B} | | RC | 3 |
| data{0:2}[15:0] | | O | I{0:1} | | | I[15:8] | RC | 9 |

Figure 12

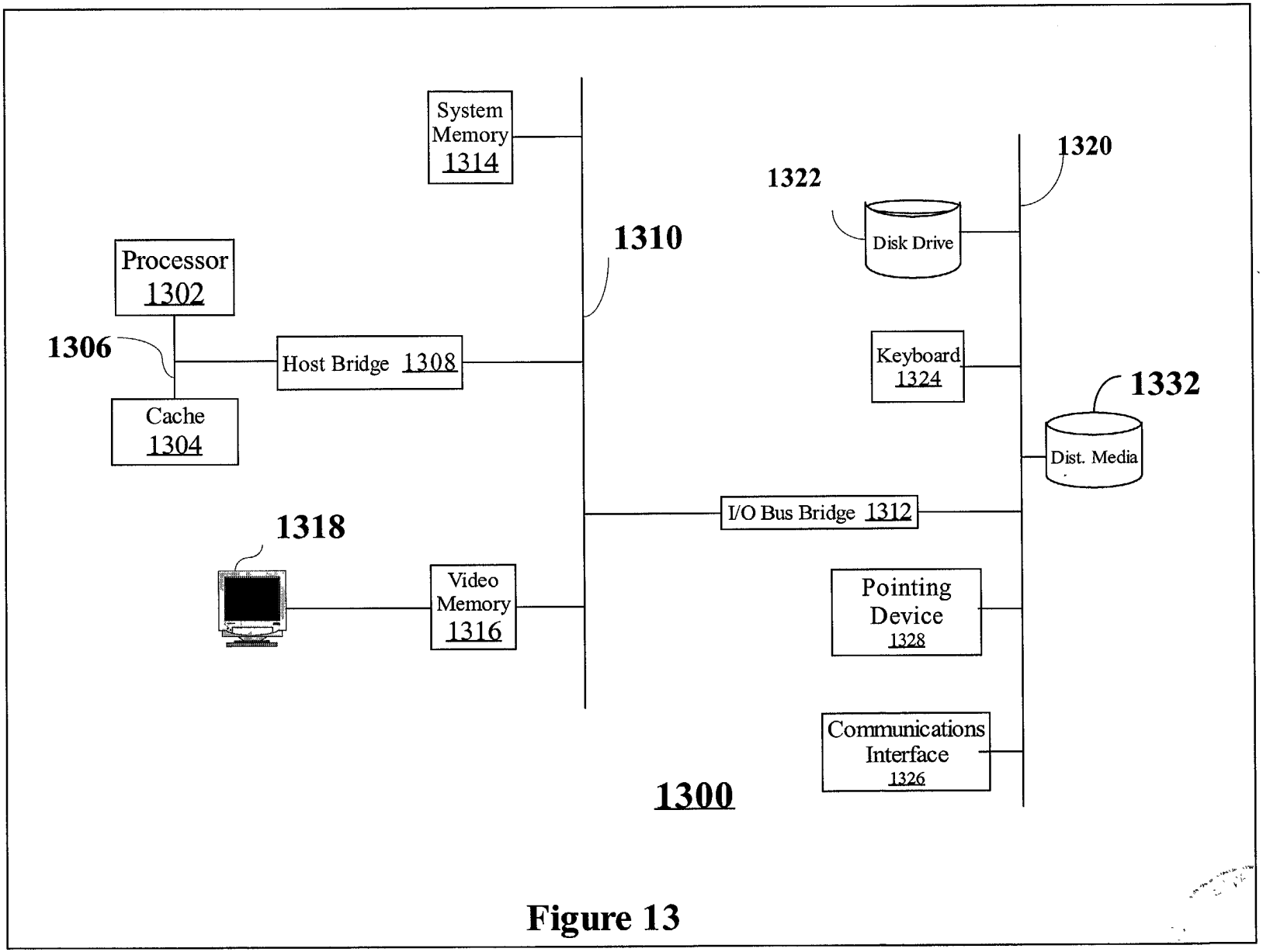

System Memory 1314
1310
1320
1322
Disk Drive
Processor 1302
1306
Host Bridge 1308
Keyboard 1324
1332
Dist. Media
Cache 1304
I/O Bus Bridge 1312
1318
Video Memory 1316
Pointing Device 1328
Communications Interface 1326
1300

Figure 13

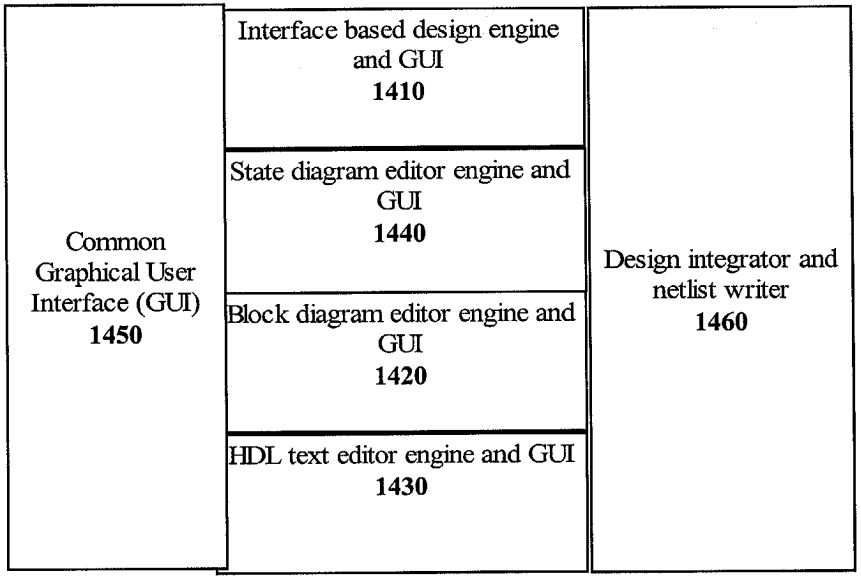

Common Graphical User Interface (GUI)
1450
Interface based design engine and GUI
1410
State diagram editor engine and GUI
1440
Block diagram editor engine and GUI
1420
HDL text editor engine and GUI
1430
Design integrator and netlist writer
1460

Figure 14

| | | ModuleName |
|---|---|---|
| myBundle | data[32] | B |
| | R/W* | I |

1510

Figure 15

| | ModuleName |
|---|---|
| myBundle | * |

Figure 16